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abakadaunanghakbangsapagbasabookfreedownload abakadaunanghakbangsapagbasabookfreedownloadThe present invention relates to stacked-capacitor memory and more specifically relates to semiconductor read only memory (ROM). Semiconductor ROMs use active elements such as transistors, diodes, and bipolar junction transistors as memory cells. To reduce the area requirements of these cells, many semiconductor ROM designers have selected planar or buried channel transistors. This, in turn, normally requires the construction of arrays of select lines in the array of memory cells. Select line structures with decreasing critical dimensions (e.g., channel length) are being used to save space and increase the density of the arrays of memory cells. One problem that can occur in the manufacture of small critical dimension ROM devices is that a shorter select line can give rise to undesirable electrical properties in select devices associated with the select line. Because of these problems, the use of self-aligned lateral double-diffused (xe2x80x9cSLDDxe2x80x9d) MOS ROMs has become widespread. In a typical layout of the arrays of memory cells, the center-toward-edge select lines are referred to as a driver element and the drain-

source shorting line (or SGND) serves as a discharge line of the floating gate of the memory cell. The drain-source shorting line of one memory cell is connected to the SGND of the next memory cell. A self-aligned memory cell can be formed by first providing a channel region of a drain-source region of a MOS transistor. A portion of the channel region is masked and a portion of the channel region is doped in the substrate. The doped portion of the channel region is referred to as the LDD region. In a self-aligned memory cell the minimum possible LDD length of the drain and source regions (which define the maximum potential differences between the two regions) are the same, which is inversely related to the transistor width. However, a problem of a standard self-aligned ROM cell is that the LDD region covers the entire sidewall of the MOS transistor. A large LDD region that covers the entire sidewall of the MOS transistor requires the use of a thick gate oxide, which in turn reduces the gate-to-substrate capacitance. This in turn reduces the effectiveness of the select transistor c6a93da74d